Remarks

Applicant and the undersigned would like to thank the Examiner for his guidance and efforts in the examination of this application, and for consideration of the claims remaining in the Request for Continued Examination case. Claims 1, 2, 6, 7, 11 -13, 15, 19, and 20 remain in the case. Claims 8 - 10are cancelled by this amendment. New claims 21 - 23 are added. No new matter is added by this amendment.

Claims 1,2, 6 - 13, and 15, 19, and 20 were objected to because of informalities. Claims 1,6 - 10, 11 - 13, 15, 19, and 20 were rejected under 35 U. S.C. § 103 (a) as being unpatentable over Yatsuda '444 in view of Chung '650.

Reconsideration is respectfully requested in view of the above amendments and arguments herein presented.

The Examiner rightfully points out that Yatsuda '444 teaches a process of making a flip-chip SAW which comprises steps of forming a material having a first and second surface and a cavity with a recess to receive a lid and sealing the lid in the recess over the inserted SAW die. However, Yatsuda '444 does not teach the array processing of hermetically sealing the flip-chip SAW devices. Specifically, Yatsuda '444 disclsoes a singulated SAW device in which the cavity extends from the first surface to the other side of the second surface creating two openings for the SAW package. The two openings allows for a mounting of the SAW die in a flip chip arrangement in one cavity and does tuning through the other cavity window (see 12e of Fig 1). Thus, the recess formed in the cavity as depicted in Fig.1 of Yatsuda '444 is for the sole purpose of creating a window through which an etching gas can be passed to adjust the characteristics of the SAW die after it is assembled (see Column 5 lines 7 -16 and Column 6 lines 42 - 46 by way of example). A method of processing a singulated SAW flip-chip device is considered as prior art in specification as originally filed (see Column 2 lines 20 - 25 of the published application). Respectfully, the present invention is

directed to a method of array processing of hermetically sealed SAW flip-chip devices in which the recess in the cavity becomes the enabling technique for the array processing of solder reflow without bridging between the lids. Yatsuda '444 neither discloses nor suggests such a teaching.

Further, while Chung '650 teaches a process for a plurality of optical devices including providing each lid over each inserted optical devices and separating the wafer into individual optical device, the sealing of the lid over each optical device results in a non-hermetically sealed structure. Chung '650 teaches the application of a wet adhesive preformed to the transparent covers in pre-determined locations and the covers are then B-staged or dried. The sheet of optical devices is singulated into individual devices. It is agreed that such a method is well known as indicated to the specification as originally filed (see Column 2, lines 6 - 18 of the published application by way of example). As supported by the specification and as taught by the Applicant, this would be a drawback when sealing the SAW die because such a seal as suggested by Chung '650 is inherently non-hermetic and would allow certain gases especially water vapor to permeate into the cavities. Claimed embodiments of the present invention includes an array process of hermetically sealing SAW die in a flip-chip arrangement using metal lids and solder reflow process or ceramic lids and glass frits sealing techniques (see Column 1, lines 16 - 22).

By way of further support for allowance of the claimed invention, Chung '650 teaches away from both these processes, stating that solder sealing process is inconvenient or impractical because of the adverse effects on the devices that result from the high temperatures required for making soldering attachments (see Column 1 lines 52 - 56 of Chung by way of example). The Chung '650 further states that the hermetically sealed packages are very expensive to fabricate (Column 1 lines 65 - 68). Chung '650 also points out that the glass sealing technique is long and sensitive. The temperature coefficients of expansion of the glass frit, the lid, and the package have to

be well matched (see Column 2, lines 4 - 22).

Yet further, the Yatsuda '444 reference does not teach the array processing of hermetically sealed SAW flip-chip devices and does not teach nor suggest the hermetically sealing the lids within the recesses formed in the array cavities. By way of example, and as supported by the specification (page 2, beginning Line 3), the technique of externally fixturing solder lids onto an array is very difficult to accomplish due to the small dimensions of the flip chip SAW devices. As those of skill in the art will appreciate, the small dimensions of the lids, the limited clearance between packages on the array, and the camber of the array make it difficult to maintain integrity between the external fixture and the array during solder reflow. Yatsuda '444 does not teach nor suggest a solution to overcome this problem associated with the array processing of hermetically sealed SAW flip-chip devices. By way of example, the recess depicted in Figure 1 of Yatsuda '444 is solely for the purpose of creating a window through which a tuning process can be accomplished. Again, Chung '650 teaches an array processing of optical devices using adhesive forming non-hermetic devices. In comparison, Chung '650 actually discourages the techniques as taught in the claimed invention, stating that it is inconvenient, impractical, delicate and expensive. Respectfully, with such a teaching away, it would not be obvious to one skilled in the art to provide the claimed inventions having using the teachings of Yatsuda and Chung. It is only through the teachings of the Applicant that a person of ordinary skill in the art would arrive at the teaching of this invention including the process of hermetically sealing the SAW flip-chip die within each cavity of the array for providing the devices for the purpose of optimizing production to reduce cost and time.

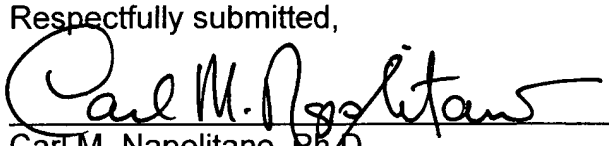
Claims 2 and 7 are rejected as being unpatentable over Yoshimoto et al in view of Chung and further in view of Yoshihara et al. Yoshimoto '129 teaches a method of assembling bulk wave piezoelectric oscillator in an array of resinous packages. Since the package is resinous, it is well known that it would not provide a hermetic seal and

would allow certain gases such as water vapor to pass through. Further, Yoshimoto teaches assembling of bulk wave devices and not surface acoustic wave devices. Yoshimoto does not teach nor suggest sealing of the devices in a hermetic manner using metal lids with solder reflow or ceramic lids using glass sealing technique as disclosed in the invention. As mentioned above Chung teaches away from the hermetic-sealing techniques such solder and glass sealing, but teaches an array processing of optical devices using adhesive forming non-hermetic devices. Both Yoshimoto and Chung do not deal with miniaturized SAW flip-chip devices. Therefore, claims 2 and 7, depending from claim 1, would appear to clearly distinguish over the teachings of Yoshimoto and Chung.

New claims 21 - 23 are fully supported by the specification as originally filed and are herein presented to claims to alternate embodiments of the invention.

Therefore, Applicant respectfully submits that the above amendments place this application in a condition for allowance, and passage to issue is solicited. The Applicant and the undersigned would like to again thank the Examiner for his efforts in the examination of this application and for reconsideration of the claims as amended in light of the arguments presented. If the further prosecution of the application can be facilitated through telephone interview between the Examiner and the undersigned, the Examiner is requested to telephone the undersigned at the Examiner's convenience.

Respectfully submitted,



Carl M. Napolitano, Ph.D.
Reg. No. 37,405
ALLEN, DYER, DOPPELT, MILBRATH & GILCHRIST, P.A.
255 South Orange Avenue, Suite 1401
P.O. Box 3791
Orlando, Florida 32802
(407) 841-2330
Agent for Applicant